Electrical stability and thermal annealing effects in pentacene thin film transistors passivated by parylene

S. Cipolloni, D. Simeone, L. Mariucci*, A. Pecora, L. Maiolo,
M. Cuscunà, A. Minotti and G. Fortunato

IFN-CNR, Via Cineto Romano 42, 00156 - Roma (ITALY),
*tel.: + 39 06 41522229; fax: + 39 06 41522220; e-mail: mariucci@ifn.cnr.it

We studied the electrical characteristics of pentacene TFTs fabricated by using a parylene film as passivation layer in order to define the device active area through conventional lithographic process. Passivated devices have been thermal annealed at different temperatures, improving the pentacene structure. The electrical characteristics of annealed TFTs have been measured under different ambient conditions and their electrical stability under bias stress condition has been evaluated.

1. Introduction

In the last decade organic thin film transistor (O-TFTs) have attacted a considerable interest, thanks to their low cost, low temperature process and mechanical flexibility. At present, the best results have been shown for pentacene-based TFTs, fabricated on a variety of substrates and dielectric layers. Recently, a number of authors have reported high performance pentacene transistors, comparable with amorphous silicon TFTs[1-3].

Patterning is a crucial part of the fabrication of OTFTs. In fact, organic semiconductor must be defined into the active layer island, to eliminate parasitic leakage currents and reduce cross-talk. Moreover, the active layer must be encapsulated because the exposure to air can induce degradation of pentacene film[4] with consequent modifications of the electrical characteristics. Unfortunately, pentacene is not compatible with organic solvents, which are normally used in the fabrication process, moreover, the exposure to air or high temperatures (more than 70°) is in general detrimental to the device performance.These limitations are responsible for the difficulties encountered with patterning and encapsulation steps. Therefore, one of the main challenges, related to the processing of organic semiconductor, is the possibility to find a protective coating enabling patterning of the active layer as well as preventing aging effects caused by air and humidity.

The use of conventional optical lithography to pattern pentacene active layers has been already demonstrated, in combination with different passivation film, including PVA [5], parylene [6].

In this work, we present high-performance pentacene TFTs fabricated using a parylene film as passivation layer, enabling a subtractive processes to define the active layer. In particular, we show an experimental study of the thermal annealing effects on the TFT characteristics, measured under different ambient, and their electrical stability.

2. Device fabrication

Bottom contact devices (BC) have been fabricated on heavily doped silicon wafers (acting as gate electrode), with thermal silicon dioxide, 90 nm thick, as gate dielectric. Source and drain gold contacts, 20 nm thick, are defined using optical lithography and wet-etching (W=195 μm , L=23 μm). A thin film of polycrystalline pentacene (Sigma Aldrich , 99% purity) , 30 nm thick, has been evaporated on the PMMA buffer layer used to improve the structural properties of pentacene (a more detailed description of the use of PMMA as buffer layer can be found in Ref. 7). A 0.5 μm thick layer of Parylene-C (poly-para-xylylene) is then deposited by Chemical Vapor Deposition (CVD) in vacuum and at room temperature. Then the photoresist (Shipley 1813) is spun on top of the structure and cured at 60°C for 10 minutes. The sample is exposed to UV radiation through a lithographic mask and subsequently developed. The structure is then dry etched in oxygen plasma.

3. Experimental results

Transfer characteristics have been measured in vacuum (P=0.1 mbar) and at V_{DS}= -1V by ramping up-down the gate voltage on the same device before the parylene deposition and after the pentacene patterning. As can be seen in figure 1, there is no appreciable device degradation induced by parylene passivation and the subsequent lithographic processes except for a little increase in the subthreshold slope (from 0.25 V/dec to 0.4 V/dec). Unfortunately, parylene appeared not good enough as passivation layer, because as can be seen in Fig.1, the trasfer characteristics measured in air show a substantial degradation, if compared to those measured in vacuum, with also a dramatic increase in the hysteresis. It should be pointed out that such device degradation is perfectly reversible (not shown), as long as the sample is exposed to air for a relatively short time (few hours). In fact, when remeasuring in vacuum, the electrical characteristics are fully recovered. It can be argued that such device degradation, observed

when measurements are perfromed in air, is related to oxygen absorption and interaction with pentacene molecules. The present results suggest that oxygen can easily move through the parylene passivation layer. Therefore, although parylene is well known as an inert and chemically resistant layer, it seems not to be sufficiently good as a barrier to oxygen and, presumably, water related species. However, this can be overcome by adding, after pentacene patterning, an additional barrier layer, such as acryl [5], to reduce oxygen permeability.

In order to study aging effects, we exposed a sample to air and light for more than 6 weeks, during which it was repeatedly measured, at different aging times. Similarly to what already observed in our previous work [8], aging doesn't affect the subthreshold region, but reduces the on-current and increases the hysteresis in the up-down characteristics, with the degradation rate decreasing with aging time (not shown). In our previous work [8], we explained these effects by a band mobility reduction accompanied by defect generation. The new defects give rise to extra tail states, caused by pentacene film oxidation, whereas the deep state density, which controls the subthreshold region, remains nearly unaffected by the aging. These findings are in agreement with theoretical calculations, showing that oxygen atoms and H_2O molecules, interacting with pentacene films, induce defect levels near the valence band[9]. On the other hand, a gradual increase in the defect density must corresponds to a gradual increase in crystal distortions and scattering phenomena leading to a mobility decrease.

We then tested, on a different sample, the effects induced by thermal annealing at increasing temperatures. In Fig. 2 the transfer characteristics are reported for the same device annealed at increasing temperatures, from 70°C up to 120°C. The device was measured in vacuum (V_{DS}= -1V) after each annealing step (30 minutes). The annealing improves the field-effect mobility up to 120°C and also the hysteresis was found to slightly decrease while threshold voltage and subthreshold region remain substantially unchanged. For T=130°C no further changes were observed, if compared to the 120°C curve, while for T>140°C device degradation starts. Therefore, we established 130°C as the maximum processing temperature of all the subsequent processes following parylene passivation.

In Fig. 3 the electrical characteristics for an OTFT, after thermal annealing at 120°C, are reported. From the experimental data, a field-effect mobility (deduced from the linear regime) μ_{FE}= 0.41 cm^2/Vs , a subthreshold slope of 0.4 V/dec, a threshold voltage of - 4V and an on/off current ratio of 10^7 (between +5 and -15 V) can be estimated. In addition, the hysteresis, observed in the up-down measurements, is practically suppressed, when measuring in vacuum, and it is also substantially reduced when measuring the characteristics in air, if compared to the data reported in Fig. 1. It should be

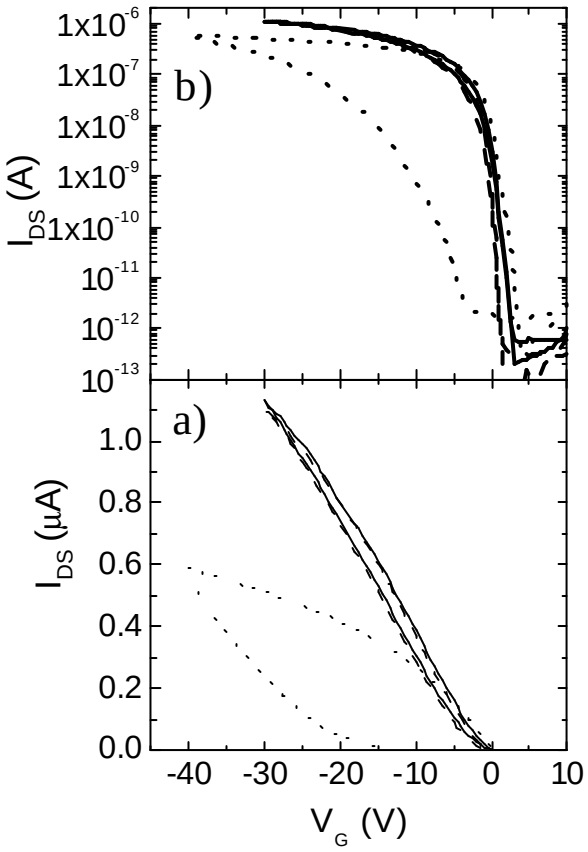

Fig. 1: *Experimental transfer characteristics, measured in vacuum ramping up-down the gate bias, before parylene deposition (solid line), after pentacene patterning (dashed line) and after pentacene patterning, measured in air (dotted line).*

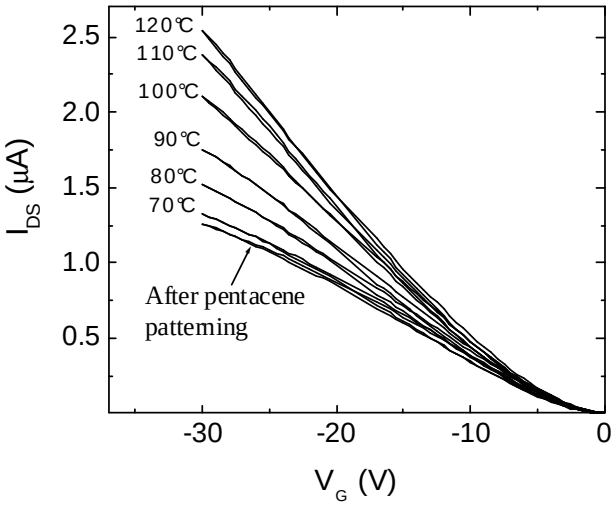

Fig. 2: *Experimental up-down transfer characteristics, measured in vacuum, aftter the pentacene patterning for different annealing temperatures.*

also mentioned that measurements performed in dry nitrogen atmosphere are exactly the same to those performed in vacuum, further confirming the role of oxygen and humidity in the degradation process.

From the present results we can conclude that the TFTs increased performances after thermal annealing could be releted to a general improvement in the structural properties (improved grain boundaries). These structural improvements are also at the basis of reduced hysteresis, as confirmed by the recent studies by Toccoli et al.[10]. In fact, it has been shown that improving pentacene film morphology leads to reduced gas sensitivity, in agreement with our results.

Finally, we studied the electrical stability after thermal annealing. It is well known [11] that negative bias stress in OTFTs shifts the threshold voltage, V_T, towards the negative voltage, while the mobility, the subthreshold slope and the on/off ratio are unaffected. These effects can arise from slow trapping in the surface states at the semiconductor/dielectric interface or from the creation of defects in the bulk[11,12]. The electrical stability of OTFTs after thermal annealing was tested by applying prolonged gate bias stress (up to 10^4 s) with negative gate voltage $V_{Gstress}$= -30 V and with V_{DS}= -1V. Transfer characteristics, monitored at selected times during the bias-stressing cycle, are shown in figure 4. As can be seen, minimal V_T shift was observed. It is interesting to compare the dynamic of the V_T shift for the present patterned and annealed devices with that relative to conventional un-passivated TFTs[11] as shown in Fig. 5. It is evident that devices after encapsulation and thermal annealing show very stable characteristics.

We also studied the electrical stability in parylene passivated devices after aging before and after thermal annealing and the results are reported in Fig. 6 a-d. It can be seen that the V_T shift in passivated devices is appreciably better than in unpassivated OTFT (see Fig. 5). Thermal annealing restores in the aged device its original characteristics and drastically reduced the V_T instability, as already observed.

4. Conclusions

Passivation of pentacene TFTs with parylene layer allows the the define of transistor active area by using standard lithographic process without an appreciable reduction of device characteristics. However, the degardation of electrical characteristics of passivated devices measured in air show that parylene layer is not an efficient barrier against oxygen diffusion and an additional barrier layer is required to reduce the instability induced by oxygen or water related species. On the other hand, the encapsulation of pentacene devices with parylene layer allows the annealing of pentacene TFTs up to 130°C, resulting in an enhancement of electrical characteristics as a consequence of improved structural properties. Indeed, annealed devices show increased field effect mobility, re-

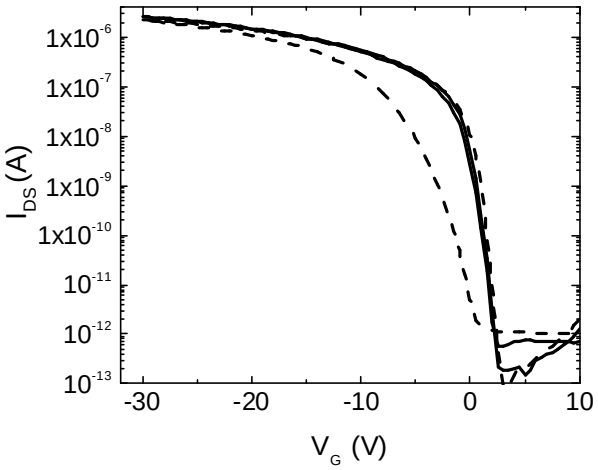

Fig. 3: *Experimental up-down transfer characteristic (V_{DS}= -1 V) of annealed device, measured in vacuum (solid line) and in air (dashed line).*

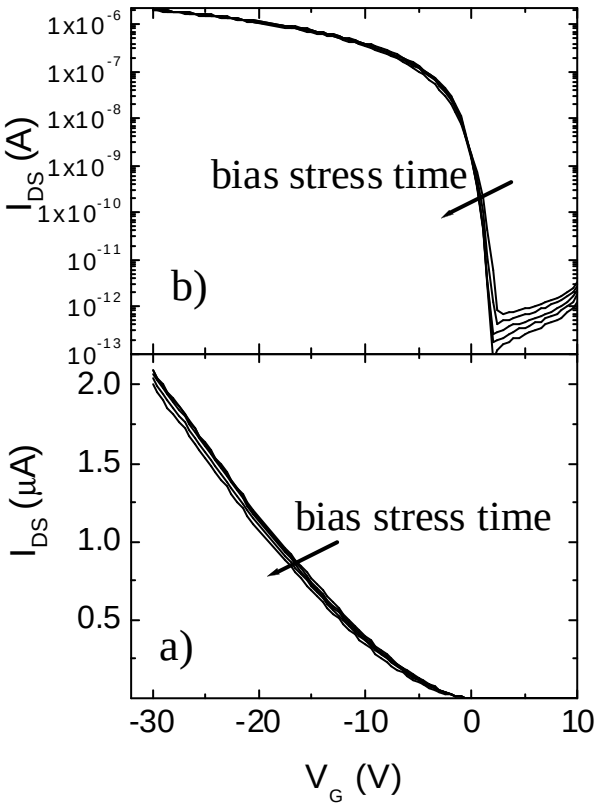

Fig. 4: *Experimental transfer characteristics measured in vacuum on pentacene patterned and annealed device at different bias stress time (0-10^4s). Bias stress condition $V_{Gstress}$= -30V , V_{DS} = -1V.*

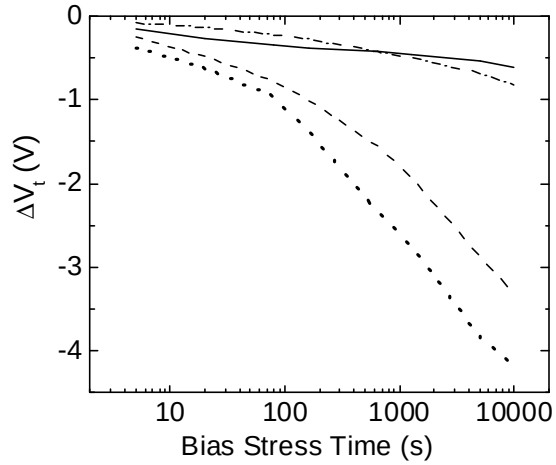

Fig. 5 *V_T shift for conventional un-passivated (dotted line), and passivated and anneled TFTs (solid line). Also shown is the V_T shift for passivated and aged TFTs before (dashed) and after (dot-dashed) thermal annealing.*

duced hysteresis and result very stable under bias stress condition with a reduced threshold voltage instability.

Acknowledgments

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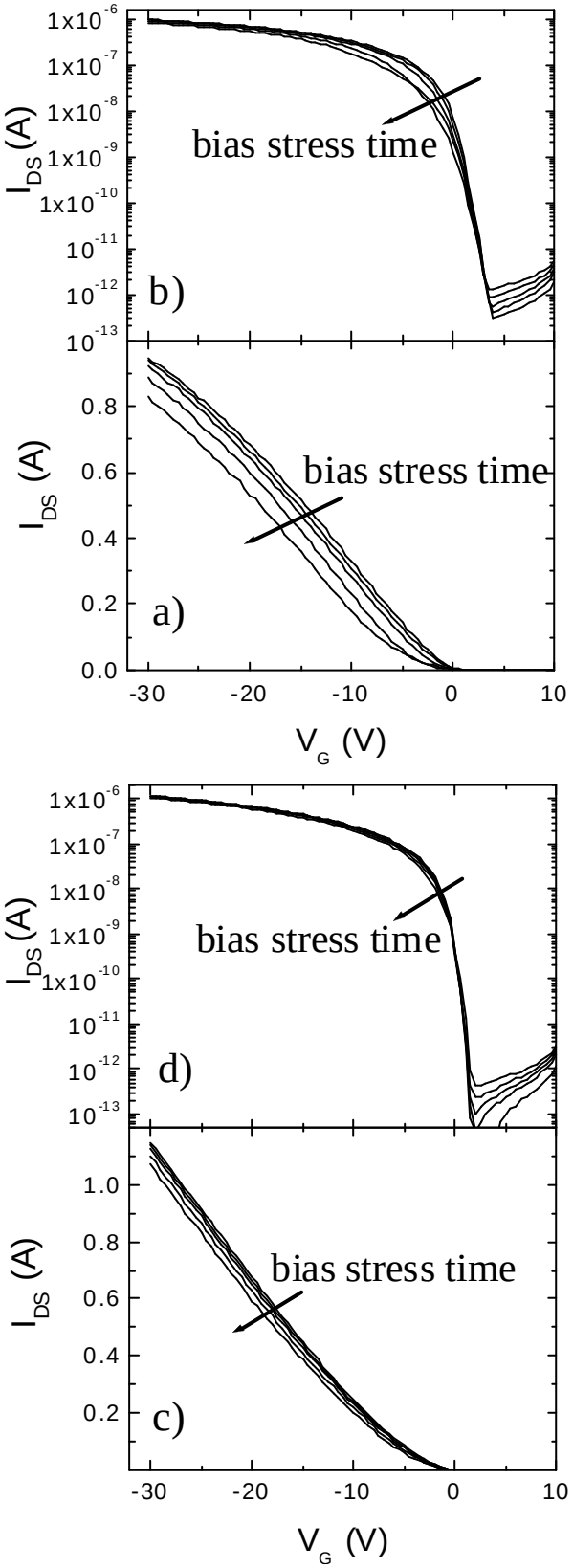

Fig. 6: *Experimental vacuum transfer characteristics measured on pentacene patterned aged and not annealed device (a-b) , and on aged but annealed device (c-d) at different bias stress time (0-10^4s). Bias stress condition $V_{Gstress}$= -30V , V_{DS} = -1V.*