Electrical stability and thermal annealing effects in pentacene thin film transistor passived by parylene

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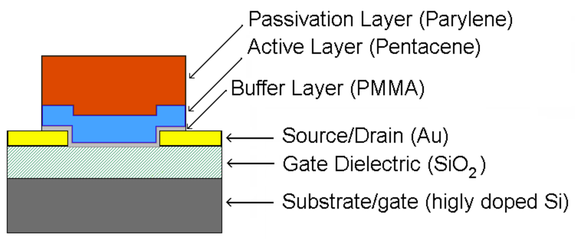
Summary

We studied the electrical characteristics of pentacene TFTs fabricated by using parylene film as passivation layer in order to define the device active area through conventional lithographic process. Passivated devices have been thermal annealed at different temperatures, improving the pentacene structure. The electrical characteristics of annealed TFTs have been measured under different ambient conditions and their electrical stability under bias stress condition has been evaluated.

Technology

Devices architecture

Pentacene –TFT with bottom contact configuration:



SUBSTRATE: highly doped silicon (gate)

DIELECTRIC: silicon dioxide 80 nm thick

SOURCE-DRAIN: gold contacts, defined by optical lithography.

L=20 μm, W=200 μm.

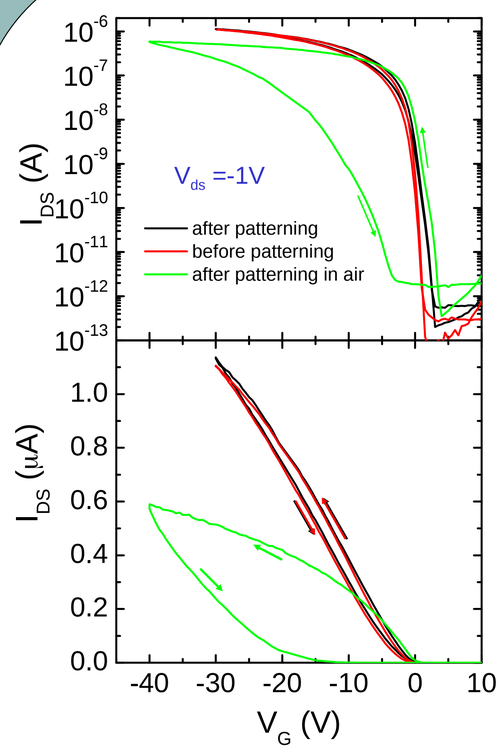
PMMA BUFFER LAYER: spin-coated, 5 nm thick, baked at 90° for 20 min.

PENTACENE: 10-100 nm thick, deposition rate 0.7 A°/s, P=10^{-7} mbar

PASSIVATION: 0.5 μm thick Parylene-C, deposited by Chemical Vapor Deposition (CVD) in vacuum and at room temperature. The structure is defined by optical lithography and then dry etched in oxygen plasma.

Electrical characterization

Transfer characteristics



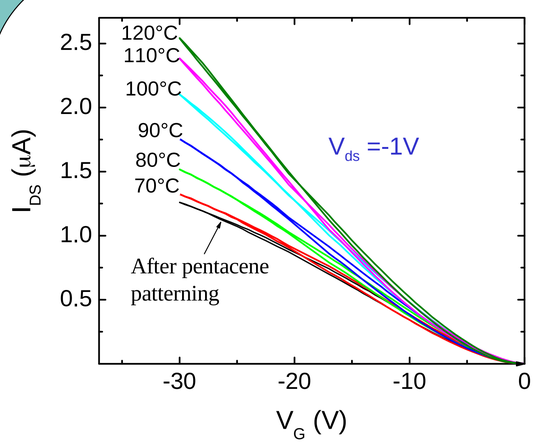
I_{DS}-V_G measured in vacuum and air, with up – down voltage ramp, before and after the pentacene patterning:

- no appreciable device degradation is induced by parylene passivation and the subsequent lithographic processes.
- field-effect mobility,, μ_{FE}= 0.2cm²/Vs, in linear regime.
- subthreshold slope= 0.25 V/dec (before passivation)
- subthreshold slope= 0.4 V/dec (after passivation)
- threshold voltage - 4V
- on/off current ratio 10^7 (between +5 and -15 V)

- parylene appeared not good enough as passivation layer: the transfer characteristics measured in air show a substantial degradation, if compared to those measured in vacuum, with also a dramatic increase of the hysteresis.

- device degradation and hysteresis effect, observed in air, are fully reversible when the vacuum conditions are restored.

Thermal annealing effects



Transfer characteristics, measured in vacuum, of a device annealed at increasing temperatures, from 70°C up to 120°C.

Parylene passivation allows thermal annealing of pentacene TFTs

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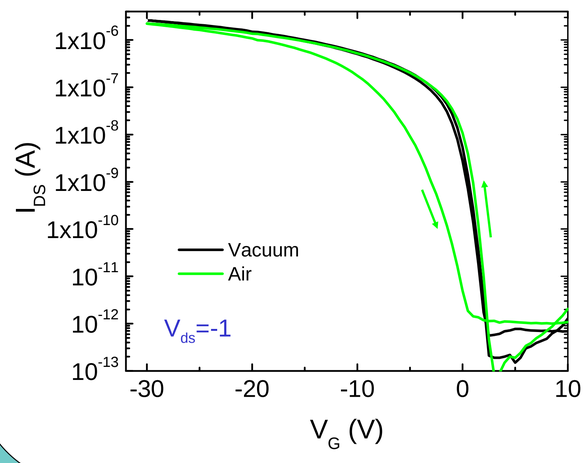
Thermal annealing:

- progressively improves field-effect mobility
- decreases hysteresis of characteristics
- threshold voltage and subthreshold region remain substantially unchanged.

- For T_{ann}>140°C device degradation starts.

Transfer characteristics after thermal annealing at 120°C



- field-effect mobility, in the linear regime, μ_{FE}= 0.41cm²/Vs
- subthreshold slope of 0.4 V/dec
- a threshold voltage of - 4V
- on/off current ratio of 10^7 (between+5 and -15 V)

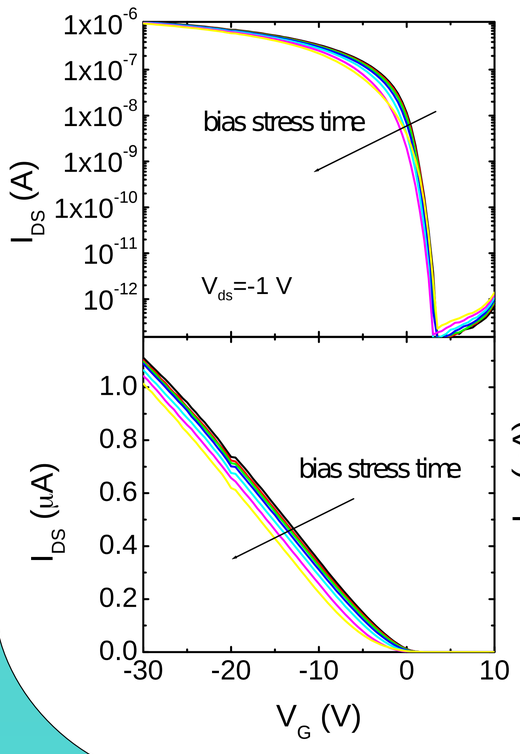
the hysteresis, observed in the up-down measurements, is:

- practically suppressed, when measuring in vacuum
- it is substantially reduced when performing the characteristics in air

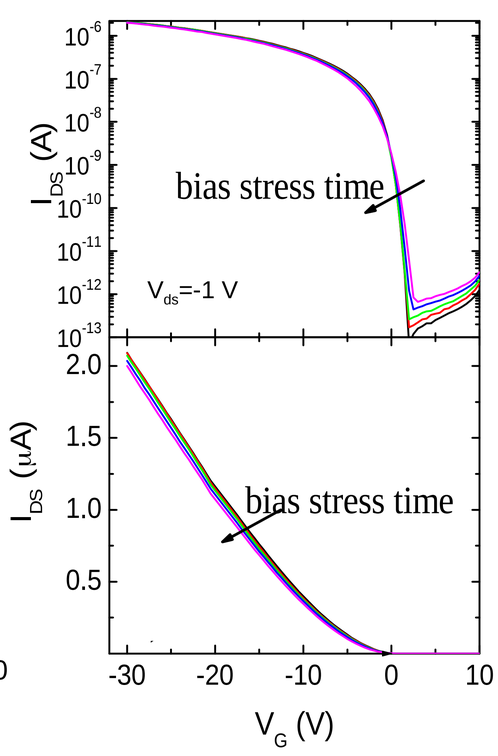
Electrical stability before and after annealing at 120°C

Bias stress condition: $V_{Gstress}$= -30V ,V_{DS} = -1V, bias stress time (0 – 10^4)s

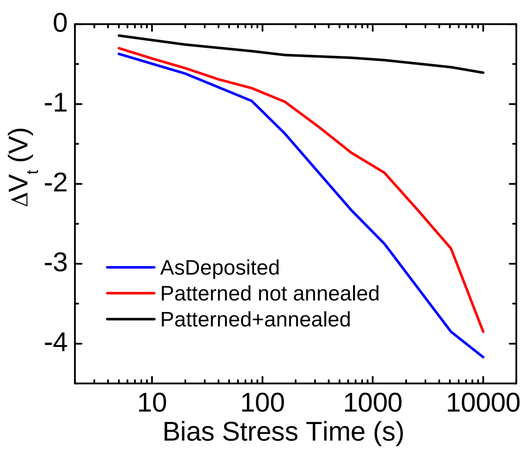
Passivated, not annealed device:
V_T shift is observed



Passivated and annealed device:
minimal V_T shift



Threshold voltage shift



Devices after passivation and thermal annealing show very stable characteristics under bias stress condition

Conclusions

- Passivation of pentacene TFTs with parylene layer allows to define the transistor active area by using standard lithographic process without an appreciable degradation of device characteristics.

- The degradation of electrical characteristics of passivated devices measured in air show a large hysteresis, suggesting that parylene layer is not an efficient barrier against oxygen/moisture diffusion.

- The encapsulation of pentacene devices with parylene layer allows the annealing of pentacene TFTs up to 130°C, resulting in an improvement of electrical characteristics (increased μ_{FE}), a reduced hysteresis under vacuum and air measurement conditions and an increased electrical stability under bias stress.