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Pentacene TFTs with parylene passivation layer

D. Simeone, S. Cipolloni, L. Mariucci *, M. Rapisarda, A. Minotti, A. Pecora, M. Cuscunà, L. Maiolo, G. Fortunato

CNR-IMM, via del Fosso del Cavaliere 100, 00133 Roma, Italy

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ABSTRACT

We have fabricated bottom contact pentacene TFTs on flexible polyimide substrate and silicon substrate using different passivation layers in order to reduce the electrical instability of pentacene devices, induced by water diffusion in the film, as evidenced by electrical measurements under different environments. Experimental data show that parylene passivation layer does not introduce appreciable degradation of device characteristics and allows standard lithographic process, but it is not an effective barrier for water diffusion. The encapsulation of pentacene TFTs with an additional acryl layer does not reduce the device sensitivity to the water, whereas devices encapsulated by a parylene/acryl/aluminum triple layer do not show increase of transfer characteristics hysteresis when measured in air.

1. Introduction

Pentacene thin film transistors have been widely investigated in the last decade due to their high performance, comparable to amorphous silicon TFTs [1–3], and low temperature process that enable device fabrication on plastic substrates. Two of the main issues in the fabrication of pentacene TFTs are patterning and encapsulation of devices. In fact, the definition of active layer island, required in order to eliminate parasitic leakage currents and reduce cross-talk, is difficult due to the sensitivity of pentacene to organic solvents, normally used in the fabrication process. In addition, the exposure to air or high temperatures is in general detrimental for the device performance. The use of conventional optical lithography to pattern pentacene active layers has been already demonstrated, in combination with different passivation films, including PVA [4] and parylene [5]. Passivation layers are also required in order to prevent the degradation of pentacene film induced by the exposure to air [4] with the consequent modifications of the electrical characteristics [6]. Indeed, transfer characteristics show large hysteresis when the devices are measured in air [7–9] and degradation when exposed to air for long time [10,11]. The origin of these electrical instabilities has been ascribed to oxygen and/or water absorption in the organic film and related to charge injection into gate dielectric [12] and charge trapping in the semiconductor or at the dielectric/semiconductor interface [8,13].

In this work, we present pentacene TFTs fabricated on flexible substrate using a parylene film as passivation layer, enabling photolithographic processes. Different barrier layers have been investigated in order to avoid instability induced by moisture.

2. Device fabrication

We have fabricated bottom contact pentacene TFTs on two different substrates: thermally oxidised silicon wafers and thin flexible polyimide film.

Extended gate devices have been fabricated on heavily doped silicon wafers (acting as gate electrode), with thermal silicon dioxide, 90 nm thick, as gate dielectric. Source and drain gold contacts, 20 nm thick, are defined using optical lithography and wet-etching (W=200 μm, L=20–100 μm). A thin film of polycrystalline pentacene (Sigma Aldrich, 99% purity), 100 nm thick, has been evaporated on a PMMA buffer layer (more details can be found in Ref. [14]).

Pentacene TFTs on plastic substrate (see Fig. 1) have been obtained by using a fabrication method developed for low-temperature poly-Si TFTs on PI layers [15]. Similar fabrication methods on polyimide layer has been proposed by Philips Res and applied to fabricate amorphous silicon TFTs [16]. The fabrication process starts from the spin coating of Hd 2611 polyimide on a silicon dioxide. Polyimide film (8 μm thick) was cured at 350 °C in a nitrogen atmosphere. Cured polyimide has a low CTE of about 3 ppm/°C, which closely matches that of silicon substrate. This low thermal expansion does not produce significant mechanical stress upon heating and cooling, avoiding cracking of the upper layers during the subsequent process steps. After polyimide curing, deposition of two different capping layers on PI is performed: a 50 nm film of silicon nitride deposited at 300 °C by using a dual frequency plasma enhanced chemical vapour deposition (PECVD) to improve the adhesion of following layer, and a silicon oxide film of about 160 nm, deposited at 250 °C by an electron cyclotron resonance ECR-PECVD system to protect PI against moisture and liquid chemicals. Fig. 1 shows a cross sectional view of a bottom contact pentacene OTFT used in the present work. A gate electrode, consisting of 50 nm-thick Cr, was evaporated by electron gun on the substrate, and then patterned by photolithography. A 140 nm-thick SiO_2

* Corresponding author.
E-mail address: luigi.mariucci@cnr.it (L. Mariucci).

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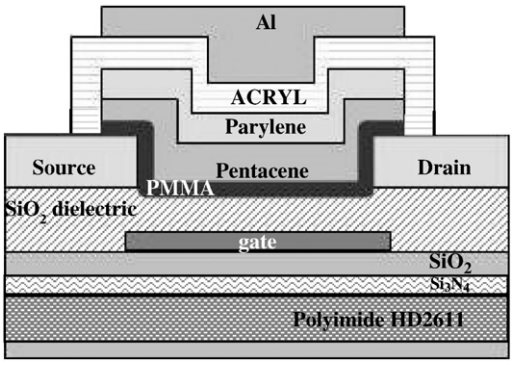

Fig. 1. Cross sectional view of a bottom contact pentacene OTFT fabricated on polyimide substrate.

dielectric layer was deposited at 250 °C on the gate. The source and drain Au contacts (20 nm thick) were defined by photolithography before the spin coating of a thin PMMA buffer layer and the evaporation of 100 nm of pentacene active layer. In order to define the pentacene island, a 0.5 μm thick layer of parylene-C (polypara-xylylene) is deposited by chemical vapour deposition (CVD) in vacuum at room temperature. Parylene and pentacene layers were patterned by dry etching in oxygen plasma. In order to obtained a better barrier between pentacene and environment, the devices were eventually encapsulated with different barrier films. A layer of photoinitialized acryl was spun on the parylene and exposed to UV radiation to be patterned; after the development, it was cured in vacuum oven at 80 °C for 4 h. The acryl island was larger than pentacene island to encapsulate it. Finally, Al layer was evaporated and patterned to cover only the pentacene island to avoid short circuits between Au contacts and Al island. When the device fabrication is completed the PI layer can be mechanically released from the rigid carrier to obtain a flexible substrate (see Fig. 2).

3. Water-related instability in pentacene TFTs

In order to identify the main causes of electrical instability of pentacene TFTs observed when measured in air, we carried out electrical characterization of extended gate devices in different environmental conditions, with different gases and relative humidity. As can be seen in Fig. 3, devices show small hysteresis effect when measured under vacuum, dry oxygen and dry nitrogen atmospheres. On the contrary when the measurements are carried out in air or nitrogen with controlled relative humidity (RH 50% and 90%, respectively) a large hysteresis is observed. These results clearly point out that this phenomenon is related to water absorption in pentacene film, while the characteristics are unaffected by the oxygen, sometime indicated as the origin of defects and electrical instability in

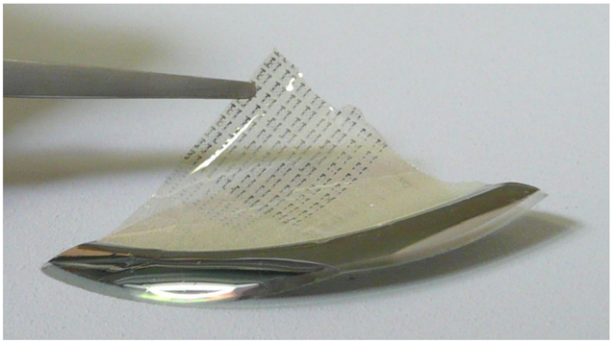

Fig. 2. Photograph of polyimide substrate with pentacene TFTs after released from the rigid carrier.

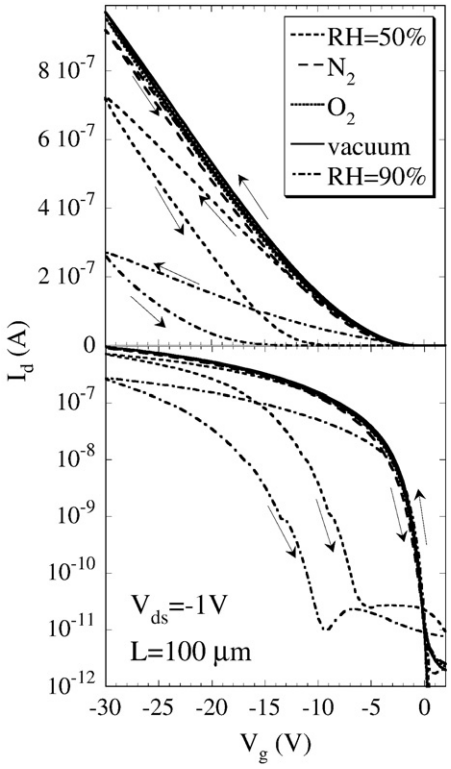

Fig. 3. Transfer characteristics of pentacene TFTs measured under different environmental conditions (shown in the label).

pentacene TFTs. Analyzing more in detail the experimental data we can observe that the off-to-on sweep of characteristic measured in air coincides with vacuum curves in subthreshold regime, but at lower V_g, in linear regime, a current reduction is observed, with an apparent decrease of field-effect mobility. During the on-to-off sweep the current remains lower than during the off-to-on sweep both in on and subthreshold regime and the on-to-off curve is almost parallel to vacuum curve in the on-region. Hysteresis effect is fully reversible when the vacuum or dry atmosphere conditions are restored indicating that the water molecules are quickly removed from the pentacene film. From the transfer characteristics is evident that hysteresis is generated from a slow variation of drain current during the measurements. In order to evaluate the time constant of the phenomenon we have measured transient drain current when the gate voltage is changed. Fig. 4 shows the drain current variation when pentacene TFT is biased at V_g=−30 V starting from V_g=0 V and when

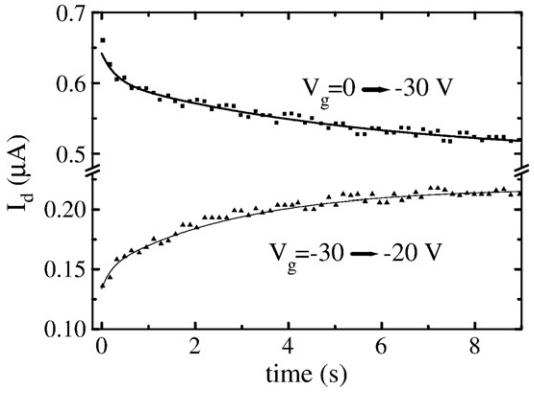

Fig. 4. Time dependence of the drain current of a pentacene TFT, measured in air, after changing gate voltage from O V to −30 V (squares) and after changing V_g from −30 V to −20 V (triangles). I_d-curves are fitted by two-exponential decay functions (solid lines).

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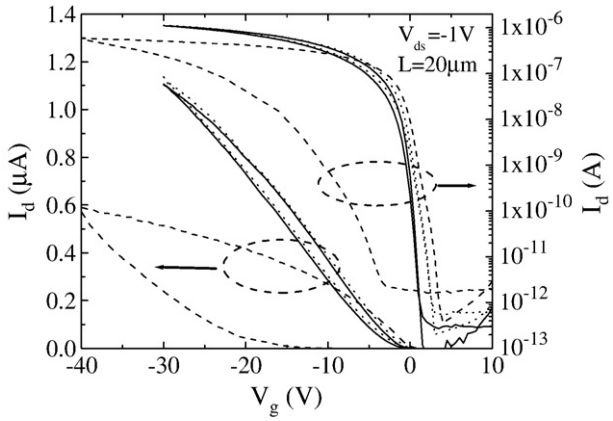

Fig. 5. Transfer characteristics of pentacene TFTs measured at V_{ds}=−1 V, sweeping gate voltage from positive to negative values and back: before parylene deposition (solid line), after pentacene patterning (dot line), both measured in vacuum, and after pentacene patterning, measured in air (dashed line).

V_g is changed from −30 V to −20 V in air condition (RH=50%). As can be seen, the drain current, during the off-to-on switch, after a fast decrease, tends to the equilibrium value quite slowly whereas during the on-to-off switch the current increase, again reaching the equilibrium value after several second. In both case the drain current variation can be fitted by the sum of two exponential decays (solid curves in Fig. 5)

$$I_d = I_0 \exp(-t/\tau_0) + I_1 \exp(-t/\tau_1) + I_2$$

where the fastest time constant, τ_0, is of the order of 0.1–0.2 s, whereas τ_1 is between 3 and 5 s for both on-to-off and off-to-on switches. These experimental results can be interpreted considering that hysteresis of transfer characteristics is induced by slow trapping of positive charge during the off-to-on sweep, with time constant comparable with the measurement time. Trapped charge is slowly released during the on-to-off sweep resulting in the observed hysteresis. Charge trapping is clearly related to water absorption in pentacene film, but the microscopic mechanism is still not clear.

4. Encapsulation of pentacene TFTs

Considering the role of the moisture in the electrical instability of pentacene TFTs it is mandatory to identify an effective barrier against the water diffusion in pentacene active layer. We have investigated organic (parylene and acryl) and inorganic (aluminium) encapsulation layers on pentacene devices.

4.1. Parylene passivation layer

As already reported in literature, parylene has been successfully used to pattern organic active layer [5,17–19] and we have tested it also as water barrier layer. Fig. 5 shows the transfer characteristics of extended gate pentacene TFTs, with parylene passivation layer, measured in vacuum (P=0.1 mbar) and air, at V_{ds}=−1 V, sweeping gate voltage from positive to negative values (off-to-on sweep) and back to positive voltage (on-to-off sweep), before and after parylene deposition and pentacene patterning. Before the parylene deposition the devices exhibit, when measured in vacuum, a typical field effect mobility of μ_{FE}=0.5 cm^2/Vs, a subthreshold slope of 0.25 V/dec, threshold voltage V_{th}~−8 V, and on/off current ratio $I_{on/off}$>10^5. After patterning, there is no appreciable device degradation induced by parylene passivation and the subsequent lithographic processes, except for a little increase in the subthreshold slope, that increases up to 0.4 V/dec, confirming that parylene is very effective as passivation layer. Unfortunately, parylene does not seem equally effective as barrier layer for water diffusion. Indeed the transfer characteristics measured in air (see Fig. 5) show a substantial degradation, if compared to those measured in vacuum, with a dramatic increase of the hysteresis effect.

4.2. Parylene/acryl passivation layer

To improve electrical stability of pentacene device we have encapsulated TFTs, fabricated on polyimide substrate, with a double layer of parylene and acryl. We note that PVA/acryl double layer has been used as encapsulation layer in pentacene TFTs [4]. Fig. 6 shows the transfer characteristics of these devices, with parylene passivation layer, before and after the spin coating and patterning of acryl layer. As can be seen, pentacene TFTs on flexible substrate exhibit, when measured in vacuum, a quite low field effect mobility (0.01 cm^2/Vs), much lower than the value measured in extended gate device, whereas the subthreshold slope (~3 V/dec) results much higher. The off current remains quite low (~10^{-12}), allowing an on/off current ratio $I_{on/off}$>10^4. The high value of the subthreshold slope can be related to an high density of localised states in the semiconductor and an high density of interface states, whereas the low field effect mobility confirm the low quality of the pentacene film. Since the pentacene of extended gate device and of TFTs on plastic was co-evaporated, the differences are probably related to the different gate dielectric. Indeed, SiO_2 deposited by ECR has an higher surface roughness compared to thermal silicon dioxide used in extended gate pentacene TFTs, possibly resulting in a lower quality of pentacene layer and of dielectric/pentacene interface. Fig. 6 also shows that, as in the case of extended gate devices, the transfer characteristics of pentacene TFTs on plastic substrate show large hysteresis when measured in air with a percentage of moisture. After encapsulation with acryl the transfer characteristics do not show degradation, indicating that parylene

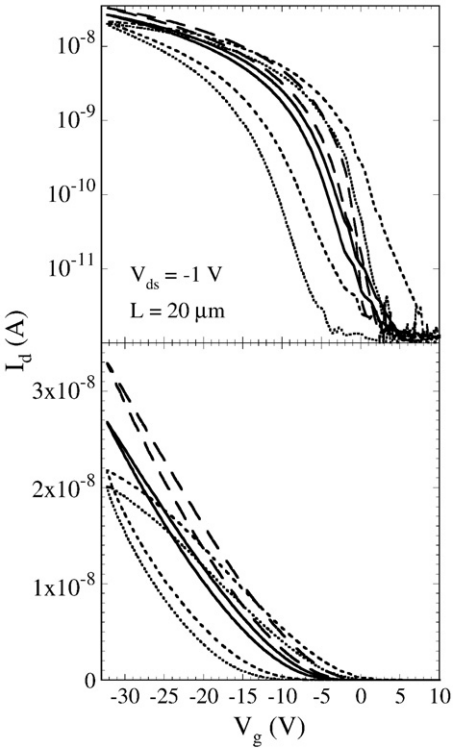

Fig. 6. Transfer characteristics of pentacene TFTs on plastic substrate measured in vacuum and air for devices without acryl layer (solid and short dashed lines) and with acryl encapsulation (long dashed and dot lines).

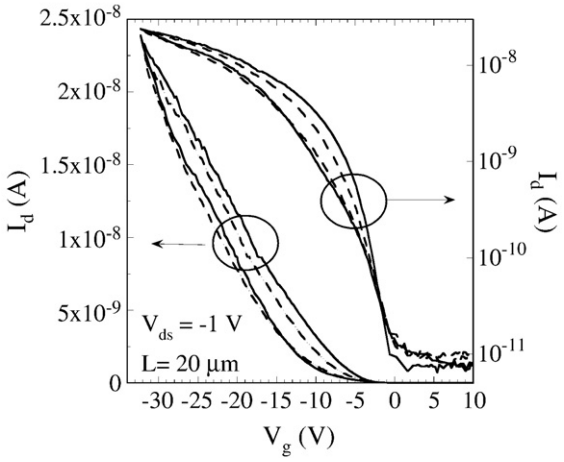

Fig. 7. Transfer characteristics of pentacene TFTs on plastic substrate, with Al encapsulation layer, measured in vacuum (solid line) and in air (dashed line).

passivation layer is quite effective in order to isolate the pentacene active layer from the solvent of acryl. However, parylene/acryl double layer is not effective as barrier layer to reduce moisture diffusion in pentacene, as evidenced from the large hysteresis of transfer characteristics measured in air.

4.3. Parylene/acryl/aluminium passivation layer

We then investigated the use of an inorganic film as barrier layer, as recently proposed by Sekitani et al. [10] who showed that Cu-layer can reduce aging effects in pentacene TFTs by reducing oxygen and water diffusion. Instead of Cu, we have used, as barrier layer, aluminium film evaporated on top of the acryl layer. The transfer characteristics of Al-passivated device, measured in vacuum, do not shown major differences if compared to the characteristics before metal passivation (compare Figs. 6 and 7), with only a small increase of hysteresis in vacuum and an increase of off-current. On the other hand, the hysteresis remains unchanged when the measurements are carried out in air, confirming that Al-layer is an effective barrier preventing water diffusion.

5. Conclusions

We have fabricated bottom contact pentacene TFTs on flexible polyimide substrate using parylene passivation layer that allows standard lithographic process without appreciable degradation of device characteristics. These devices show hysteresis of transfer characteristics, when measured in air, induced by water diffusion into pentacene semiconductor through parylene film. To improve electrical stability of pentacene TFTs we have investigated organic (acryl) and inorganic (Al) film as encapsulation layers in order to obtain an effective barrier layer for water diffusion. Both acryl and Al films can be deposited and patterned on device with parylene passivation layer without introducing appreciable variation on the device characteristics. However, whereas the hysteresis effect is still present in TFTs encapsulated with parylene/acryl double layer, the electrical characteristics of devices with a triple layer (parylene/acryl/Al) do not show increase of hysteresis when measured in air.

Acknowledgments

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References

[1] S.H. Lee, D.J. Choo, S.H. Han, J.H. Kim, Y.R. Son, J. Jang, Appl. Phys. Lett. 90 (2007) 033502.
[2] C. Rolin, S. Steudel, K. Myny, D. Cheyns, S. Verlaak, J. Genoe, P. Heremans, Appl. Phys Lett. 89 (2006) 203502.
[3] T. Toccoli, A. Pallaoro, N. Coppedè, S. Iannotta, F. De Angelis, L. Mariucci, G. Fortunato, Appl. Phys. Lett. 88 (2006) 132106.
[4] S.H. Han, J.H. Kim, J. Jang, S.M. Cho, M.H. Oh, S.H. Lee, D.J. Choo, Appl. Phys. Lett. 88 (2006) 073519.
[5] I. Kymissis, C.D. Dimitrakopoulos, S. Purushothaman, J. Vac. Sci. Technol. B 20 (2002) 956.
[6] Y. Qiu, Y. Hu, G. Dong, L. Wang, J. Xie, Y. Ma, Appl. Phys. Lett. 83 (2003).
[7] D.K. Hwang, K. Lee, J.H. Kim, S. Im, J.H. Park, E. Kim, Appl. Phys. Lett. 89 (2006) 093507.
[8] G. Gu, M.G. Kane, Appl. Phys. Lett. 92 (2008) 053305.
[9] A. Benor, A. Hoppe, V. Wagner, D. Knipp, Org. Electron. 8 (2007) 749.
[10] T. Sekitani, T. Someya, Jpn. J. Appl. Phys. 46 (2007) 4300.
[11] F. De Angelis, S. Cipolloni, L. Mariucci, G. Fortunato, Appl. Phys. Lett. 88 (2006) 193508.
[12] C.A. Lee, D.-W. Park, S.-H. Jin, I.-H. Park, J.-D. Lee, B.-G. Park, Appl. Phys. Lett. 88 (2006) 252102.
[13] J.W.H. Smith, G. Hill, J. Appl. Phys. 101 (2007) 044503.
[14] A. Pecora, L. Maiolo, M. Cuscunà, D. Simeone, A. Minotti, L. Mariucci, G. Fortunato, Solid-State Electron. 52 (2008) 348.
[15] I. French, George, Kretz, Templier, LifkaHaskal, SID Symposium Digest of Technical Papers, vol. 38, 2007, p. 1680.
[16] F. De Angelis, S. Cipolloni, L. Mariucci, G. Fortunato, Appl. Phys. Lett. 86 (2005) 086521.
[17] H. Jia, E.K. Gross, R.M. Wallace, B.E. Gnade, Org. Electron. 8 (2007) 44.
[18] K. Tsukagoshi, I. Yagi, K. Shigeto, K. Yanagisawa, J. Tanabe, Y. Aoyagi, Appl. Phys. Lett. 87 (2005) 183502.
[19] J.A. DeFranco, B.S. Schmidt, M. Lipson, G.G. Malliaras, Org. Electron. 7 (2006) 22.

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